1. (Once Amended) A method for manufacturing an interconnect structure comprising[the steps of]:

forming a recess within a dielectric material situated on a semiconductor lower substrate, said recess extending below a top surface of said dielectric material;

forming a diffusion barrier layer on the recess within the dielectric material;

forming a seed layer on the diffusion barrier layer, the diffusion barrier layer being composed of a material having a melting point greater than or equal to that of a material from which the seed layer is composed;

forming an electrically conductive layer on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

forming an energy absorbing layer on said electrically conductive layer, said energy absorbing layer having a greater thermal absorption capacity than that of said electrically conductive layer;

applying energy to said energy absorbing layer so to as heat said electrically conductive layer and to cause said electrically conductive layer to flow within said recess; and

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

2. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein [the step of] forming a diffusion barrier layer on the recess within the dielectric material is a CVD deposition step.

3. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the diffusion barrier layer is [substantially] composed is selected from the group consisting of ceramics, metallics, and intermetallics.

5. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, further comprising[the step], prior to [the step of] forming a seed layer on the diffusion barrier layer, [of] heating the diffusion barrier layer is an environment substantially containing a nitrogen gas.

6. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein [the step of] depositing a seed layer on the diffusion barrier layer is a CVD deposition step.

7. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the material from which the seed layer is [substantially] composed is selected from the group consisting of ceramics, metallics, and intermetallics.

10. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the energy absorbing layer is [substantially] composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

11. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein [the step of] applying energy to said energy absorbing layer to heat the energy absorbing layer utilizes at least one energy source selected from the group consisting of a laser, a furnace, and an RTP lamp.

12. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein [said step of] removing portions of the energy absorbing layer and the electrically conductive layer is an abrasive planarization step.

13. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 12, wherein [said step of] removing portions of the energy absorbing layer and the electrically conductive layer is a chemical mechanical planarizing step.

15. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 1, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending [substantially] parallel to the plane of the lower substrate.

16. (Once Amended) A method for manufacturing an interconnect structure comprising[the steps of]:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of the material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed;

heating the energy absorbing layer so to as heat the conductive layer and to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

20. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 16, wherein the energy absorbing layer is [substantially] composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

22. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 16, wherein the recess comprises a contact hole situated below a trench, said semiconductor substrate assembly having a lower substrate defining a plane, said contact hole terminating at an end thereof at said lower substrate and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench extending [substantially] parallel to the plane of the lower substrate.

23. (Once Amended) A method for manufacturing an interconnect structure comprising[the steps of]:

patterning and etching a dielectric material situated on a semiconductor substrate assembly so as to form a recess within the dielectric material, said recess being situated below a top surface of said dielectric material;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing an electrically conductive layer on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of a material from which the electrically conductive layer is composed, the material from which the seed layer is composed having a melting point greater than or equal to that of the material from which the electrically conductive layer is composed, the material from which the electrically conductive layer is composed is selected from the group consisting of aluminum and copper;

depositing an energy absorbing layer on said electrically conductive layer, said energy absorbing layer:

having a greater thermal absorption capacity than that of said electrically conductive layer; and

being composed of a material having a higher melting point than that of the material from which the electrically conductive layer is composed, [the

energy absorbing layer]

being is [substantially] composed of a material selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating the energy absorbing layer so to as heat the conductive layer and to cause said conductive layer to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

24. (Once Amended) A method for manufacturing an interconnect structure comprising[the steps of]:

forming a dielectric material on a monocrystalline silicon layer of a semiconductor substrate assembly, said monocrystalline silicon layer defining a plane;

patterning and etching the dielectric material so as to form a recess within said dielectric material, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said dielectric material, the trench being [substantially] parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the dielectric material, the diffusion barrier layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of ceramics, metallics, and intermetallics, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer [substantially] composed of aluminum on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum [electrically conductive layer], said energy absorbing layer:

having a greater thermal absorption capacity than that of said layer composed of aluminum; and

being composed of a material having both a higher thermal insulation capacity and electric insulation capacity than that of the layer composed of aluminum [material from which the electrically conductive layer is composed];

heating the energy absorbing layer so to as heat the layer composed of aluminum [conductive layer] and to cause said layer composed of aluminum [conductive layer] to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the layer composed of aluminum [electrically conductive layer] that are situated above the top surface of the dielectric material.

27. (Once Amended) A method for manufacturing an interconnect structure as recited in Claim 24, wherein the material from which the energy absorbing layer is [substantially] composed is selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

28. (Once Amended) A method for manufacturing an interconnect structure comprising[the steps of]:

forming at least one silicon layer on a monocrystalline silicon layer of a semiconductor substrate assembly, said silicon layer being selected from the group consisting of undoped silicon dioxide, doped silicon dioxide, undoped silicate glass, and doped silicate glass, wherein said monocrystalline silicon layer defines a plane;

patterning and etching the at least one silicon dioxide layer so as to form a recess therein, said recess comprising a contact hole situated below a trench, said contact hole terminating at an end thereof at the at least one silicon layer and terminating at an opposite end thereof at said trench, said trench extending from said opposite end of said contact hole to a top surface of said at least one silicon layer, the trench being [substantially] parallel to the plane of the monocrystalline silicon layer;

depositing a diffusion barrier layer within the recess within the at least one silicon layer, the diffusion barrier layer being composed of a material selected from the group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

depositing a seed layer on the diffusion barrier layer, the seed layer being composed of a material selected from the group consisting of aluminum, titanium nitride, titanium, and titanium aluminide, the material from which the diffusion barrier layer is composed having a melting point greater than or equal to that of the material from which the seed layer is composed;

depositing a layer [substantially] composed of aluminum on the seed layer, the material from which the diffusion barrier layer is composed having a melting point greater than that of aluminum, the material from which the seed layer is composed having a melting point greater than or equal to that of aluminum;

depositing an energy absorbing layer on said layer composed of aluminum [electrically

conductive layer], said energy absorbing layer <u>having a greater thermal absorption capacity than that of said layer composed of aluminum and</u> being composed of a material:

having both a higher thermal insulation capacity and electric insulation capacity than [that of the material from which the] <u>aluminum</u> [electrically conductive layer is composed, the material from which the energy absorbing layer is substantially composed is]; <u>and</u>

selected from the group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon;

heating the energy absorbing layer so to as heat the <u>layer composed of aluminum</u> [conductive layer] and to cause said <u>layer composed of aluminum</u> [conductive layer] to flow within said recess; and

planarizing the semiconductor substrate assembly so as to remove those portions of the energy absorbing layer and the <u>layer composed of aluminum</u> [electrically conductive layer] that are situated above the top surface of the at least one silicon layer.

Add new Claims 36-44 as follows:

36. (New) A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming an electrically conductive layer on the seed layer;

forming upon the electrically conductive layer an energy absorbing layer having a greater thermal absorption capacity than that of the electrically conductive layer;

flowing the electrically conductive layer within the recess by heat.

37. (New) The method as defined in Claim 36, wherein the melting point of:

the diffusion barrier layer is not less than that of the seed layer and is greater than that of the electrically conductive layer; and

the seed layer is not less than that of the electrically conductive layer;

38. (New) The method as defined in Claim 36, further comprising:

removing portions of the energy absorbing layer and the electrically conductive layer that are situated above the top surface of the dielectric material.

39. (New) The method as defined in Claim 36, wherein:

the electrically conductive layer is composed of aluminum; and

the energy absorbing layer is composed of a material selected from the group consisting of titanium nitride, tungsten, and a dielectric substance.

40. (New) The method as defined in Claim 36, wherein:

the electrically conductive layer is composed of copper; and

the energy absorbing layer is composed of a material selected from a group consisting of tungsten, titanium nitride, tantalum, and carbon.

41. (New) The method as defined in Claim 36, wherein:

the diffusion barrier layer is composed of a material selected from a group consisting of aluminum nitride, tungsten nitride, titanium nitride, and tantalum nitride;

the seed layer is composed of a material selected from a group consisting of aluminum, titanium nitride, titanium, and titanium aluminide;

the electrically conductive layer is composed of a material selected from a group consisting of aluminum and copper; and

the energy absorbing layer is composed of a material selected from a group consisting of titanium, titanium nitride, tungsten, tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

42. (New) The method as defined in Claim 36, wherein:

the diffusion barrier layer is composed of a material selected from a group consisting of aluminum nitride, tungsten nitride, and tantalum nitride;

the seed layer is composed of a material selected from a group consisting of aluminum, titanium, and titanium aluminide;

the electrically conductive layer is composed of a material selected from a group consisting of aluminum and copper; and

the energy absorbing layer is composed of a material selected from a group consisting of tungsten nitride, silicon nitride, silicon dioxide, tantalum, tantalum nitride, and carbon.

43. (New) The method as defined in Claim 36, wherein flowing the electrically conductive layer within the recess by heat comprises heating the energy absorbing layer with at least one energy source selected from the group consisting of a laser, a furnace, and an RTP lamp.

44. (New) The method as defined in Claim 36, wherein the seed layer comprises multiple layers, each layer in said multiple layers being composed of a material selected from the group consisting of silicon and titanium nitride.

45. (New) A method for manufacturing an interconnect structure that includes a recess extending below a top surface of a dielectric material situated on a semiconductor substrate, the recess having therein a diffusion barrier layer that is within the dielectric material, the method comprising:

forming a seed layer on the diffusion barrier layer;

forming a first layer on the seed layer;

forming upon the first layer a second layer that can absorb more heat than the first layer;

heating the first and second layers to flow the first layer within the recess by heat.